As previously discussed, independent Claims 24 and 39 recite that "the floating gate overlaps a boundary between at least one of the pair of the first impurity regions and the at least two second impurity regions." The Examiner continues to admit that Zaleski does not disclose this claimed feature but continues to cite Yamazaki and contend that it discloses a thin film transistor with at least two such second impurity regions (104 in Fig. 1 in Yamazaki) which connect source and drain regions 101 and 102. The Examiner then continues to conclude that "[i]t would have been obvious to one skilled in the art to provide Zaleski's thin film transistor with at least two such second impurity regions that connect source and drain regions 4b and 4a (resulting in a semiconductor device whose floating gate overlaps a boundary between at least one of the source and drain regions (i.e. at least one of the pair of first impurity regions) and the at least two second impurity regions) in order to suppress short channel effects as taught by Yamazaki." [Emphasis in original]. Applicant respectfully disagrees.

In Fig. 1A, Yamazaki appears to disclose a boundary between impurity region (pinning region) 104 and the source 101 or drain 102, and a boundary between channel region 103 and the source 101 or drain 102. Zaleski appears to disclose a floating gate 6 that overlaps the boundary between the channel region 4c and source 4b or drain 4a.

As Applicant previously explained, as shown in Fig. 1A of Yamazaki, the boundary between the impurity region (pinning region) 104 and the source 101 or drain 102 appears to be located apart from (or not even with) the boundary between the channel region 103 and the source 101 or drain 103. Hence, even if these two references were combinable (which Applicant does not admit), the combination would still not include the feature of "wherein the floating gate overlaps a boundary between at least one of the pair of the first impurity regions and the at least two second impurity regions" of independent Claims 24 and 39 of the present application.

In response, in the Final Rejection on page 10, the Examiner states that applicant's argument is unclear. Accordingly, Applicant is providing the following further explanation.

Initially, Applicant believes that the teachings in Yamazaki will be better understood by the Examiner by reference to Figs. 17A-17C therein. These figures show impurity regions (pining regions) 1701, 1705, 1709 are clearly located apart from potential slit region (channel region) 1704. See e.g. col. 20, ln. 61 - col. 21, ln. 13 in Yamazaki for the definition of each of these reference numerals.

In particular, at a boundary between a source region 1702 and the channel region 1704, the edge of the pining region 1701 is aligned with the channel region 1704. In contrast, at a boundary between a drain region 1703 and the channel region 1704, the other edge of the pining region 1701 is not aligned with the channel region 1704.

Further, as discussed in Yamazaki at col. 20, ln. 61 - col. 21, ln. 48 (see especially col. 20, ln. 66 - col. 21, ln. 4), "[w]ith the structure of Fig. 17A, the expansion of the drain-side depletion layer, which is a case of the punch-through phenomenon as one of the short channel effects, can be suppressed effectively. On the source region side, carriers move smoothly because the total width Wpa of potential slit region 1704 is sufficiently large." Hence, Yamazaki is stating that the pining regions increases and protrudes from the channel region (and the boundary between the channel region and drain region) in the vicinity of the drain region (so that the boundary between the pining region and the drain region is clearly separate and apart from the boundary between the channel region and the drain region). Therefore, Yamazaki clearly distinguishes the channel region from the pining region.

This is relevant to the Examiner's interpretation of Fig. 1A in Yamazaki. For example, as explained above in Figs. 17A - 17C of Yamazaki, at the boundary between the channel regions and the drain region, the channel regions are not aligned with the pinning regions. In Fig. 1A of

Yamazaki at the boundary between the channel regions and the source or drain regions, similar to the boundary between channel regions and the drain region in Figs. 17A - 17C, the channel regions are not aligned with the pinning regions.[1]

In addition, Col 8, lns. 47-56 in Yamazaki states, "In particular, it is desirable that the impurity regions 104 [pining regions] be disposed at the junction portion between the drain region 102 and the channel forming region 103 as shown in Fig. 1A, because the electric field varies the most there. Where an electric field generated by the gate voltage encompasses the drain region 102, it is preferred that the impurity regions 104 be formed so as to extend to the inside of the drain region 102. Conversely, it is preferred that the impurity regions 104 be formed so as not to extend to the inside of the source region 101" (emphasis added). Therefore, in Fig. 1A in Yamazaki, the pining regions are clearly located apart (not aligned) from the channel region.

Therefore, while Zaleski discloses that the floating gate 6 overlaps the boundary between the channel region 4c and source region 4b or drain 4a, if this reference was combinable with the teachings of Yamazaki, at most the result would be that the floating gate overlaps the boundary between the channel region and the source or drain region. Since Yamazaki does not disclose the boundary between the channel region/source or drain region and the boundary between the impurity or pining region/source or drain region as being aligned, there is nothing to teach or suggest that the combination would result in the floating gate overlapping a boundary between the source or drain regions and the pining regions. Hence, even if combined, the combination of

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[1] Col. 10, ln. 65 – col. 11, ln. 2 in Yamazaki, after the discussion of Fig. 1A in the Detailed Description of the Preferred Embodiments, states, "The invention as summarized above will be described in detail in the following embodiments. The following embodiments are merely examples of the invention, and can be modified in various manners in accordance with the needs of semiconductor device manufacturers." Therefore, Figs. 17A - 17C are variations of the structure of the pinning regions of Fig. 1A. Hence, Fig. 1A relates to Figs. 17A - 17C.

references fails to teach or suggest the claimed feature of "the floating gate overlaps a boundary between at least one of the pair of the first impurity regions and the at least two second impurity regions" of Claims 24 and 39 of the present application.

Accordingly, Claims 24 and 39 and those claims dependent thereon are patentable over the cited references, and it is respectfully requested that this rejection be withdrawn.

Claims 29, 30, 33, 34, 35, 38, 44, 46, 48, 49, 51, 53, 55, 56, 58 and 59

The Examiner also continues to reject Claims 29, 30, 33, 34, 35, 38, 44, 46, 48, 49, 51, 53, 55, 56, 58 and 59 under 35 USC §103(a) as being unpatentable over Zaleski et al. together with Yamazaki et al. and Liu (US 5,814,854). This rejection is also respectfully traversed.

For similar reasons to those discussed above, independent Claims 29, 34, 44 and 49 and those claims dependent thereon are also not disclosed or suggested by the cited references but are patentable thereover.

Accordingly, it is respectfully requested that this rejection be withdrawn.

Conclusion

Accordingly, it is respectfully submitted that the present application is in a condition for allowance and should be allowed.

If any further fee is due for this response, please charge our deposit account 50/1039.

Favorable reconsideration is earnestly solicited.

Respectfully submitted,

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